portion of said conductive material in said second, inner groove.

REMARKS

Applicant requests permission to substitute the enclosed formal drawings for the originally filed informal drawings. Applicant brings to the Examiner's attention that reference number 40 is being added to Figure 5. Page 8, line 4 of the specification refers to epitaxial layer 40. Thus, this correction to Figure 5 merely brings the drawings into conformance with the written specification.

Applicant also brings to the Examiner's attention that originally filed Figure 3 has been modified to eliminate an inconsistency. In Figure 3, there is a region of silicon dioxide above source region 21b between the oxide covering the transistor gate and contact 19. However, a similar silicon dioxide region is not illustrated above source region 21a. Applicant has eliminated this extra silicon dioxide region above source region 21b to eliminate this inconsistency.

The Examiner issued a restriction requirement and has required affirmation of Applicant's election to prosecute Claims 8 to 11. Applicant hereby affirms this election, without prejudice to Applicant's right to prosecute nonelected claims in a later filed divisional or continuation application.

The Examiner has objected to the oath as being informal. Specifically the Examiner states that the oath "lacks authentication by a diplomatic or consular officer of the United States; 37 CFR 1.66(a). This informality can be overcome either by forwarding the original oath to the appropriate officer for authentication or by filing a declaration (37 CFR 1.68) . . ." Applicant filed a "Declaration for Patent Application" with the above Application and not an oath. Thus,

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the Examiner's objection to the oath is misplaced because there was no oath. Applicant's filing of a declaration was made pursuant to Rule 37 CFR 1.68 which specifically allows for declarations in lieu of oaths. There is no requirement in the rules that declarations be authenticated by diplomatic or consular officers.

The Examiner has objected to the specification "as failing to provide best mode of carrying out invention. The process of making connection to the doped polysilicon filler is not described at all." Applicant respectfully traverses this rejection. The specification states

> Polycrystalline silicon layer 33 is then subjected to a CF_4 etch or another etch technique without using a mask in the trenched area . . . (except for a mask (not shown) which may be placed at any convenient point along the length of groove 31 in order to keep a contact pad (not shown) to the to-be--formed gate 34 shown in Figure 4e) . . . . (Page 6, lines 21 to 26, emphasis added.)

Thus, Applicant teaches a process in which a gate contact pad is formed by protecting a portion of polycrystalline silicon 33 during the CF_4 etching process. Thus, the "process of making connection to the doped polysilicon filler" is described in the present application.

The Examiner states

> The term "MOS gated SCR" is confusing. Prior art does not provide any supporting evidence that such a four layer pnpn structure would function as a SCR.

Applicant respectfully traverses this rejection. Attached Figure A schematically illustrates an MOS-gated SCR, which includes a NPN transistor Q1, PNP transistor Q2, and MOS transistor Q3. P+ substrate 41 of Figure 8 serves as the emitter of transistor Q2, N- epitaxial layer 11 serves as the base of transistor Q2, the collector of transistor Q1, and the drain of transistor Q3, P type body regions 20a and 20b serve as the collector of transistor Q2, the base of transistor Q1, and the

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body of transistor Q3, and N+ regions 21a and 21b serve as the emitter of transistor Q1 and the source of transistor Q3. Resistor R models the bulk resistance of the portion of P region 20a under source 21a and the portion of P region 20b under source 21b. When a voltage is applied across leads 50 and 51, and transistor Q3 is turned on, current flows through transistor Q2, which in turn flows into the base of transistor Q1. This causes transistors Q1 and Q2 to latch up as an SCR. Thus, the four layer pnpn structure of Figure 8 does function as an SCR. MOS-gated SCR's are described in "MOS Thyristor Improves Power-Switching Circuits" by Al Pshaenich, published in Electronic Design on May 12, 1983, attached hereto.

The Examiner has rejected Claims 9 and 11

> as being of improper dependent form for failing to further limit the subject matter of a previous claim. The claims 8 and 10 are to a MOSFET formed in groove. By forming a p+ layer instead of n+ layer as claimed in claims 9 and 11 the device transforms to a four layer power device.

Applicant traverses this rejection. Claims 8 and 10 are each directed to a "method for making a semiconductor device." Claims 8 and 10 are <u>not limited</u> to processes for making only a MOSFET. Processes for making the devices illustrated in Figures 7 and 8 come within the scope of Claims 8 and 10, and therefore, Claims 9 and 11 do properly further limit the subject matter of Claims 8 and 10.

The Examiner has rejected Claims 8 and 10 as being unpatentable over admitted prior art in view of Kazuya. The Examiner states:

> The admitted prior art lacks anticipation only in filling up the groove with polysilicon and planarizing it. It is noted that polysilicon gate is formed over gate oxide on groove sidewalls. Kazuya teaches the planarization of U-grooves by filling up with doped polysilicon, etching the upper layer polysilicon and subsequently oxidizing polysilicon. So it would be obvious to one of ordinary skill in the art to use Kazuya's

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planarization process in admittedly prior U-groove FET process since it will provide a smooth substrate surface.

Applicant respectfully traverses this rejection. Kazuya has absolutely no relevance to processes for manufacturing gates. Applicants have obtained a translation of the Kazuya reference, a copy of which is enclosed for the Examiner. As can be seen, Kazuya pertains to the formation of an isolation structure. Kazuya merely etches a groove in a silicon substrate, forms a doped channel stop region on the bottom of the groove, forms an insulating layer on the inner wall of the groove, and fills the groove with polycrystalline silicon. However, Kazuya only does this to isolate semiconductor structures formed in an integrated circuit. Nowhere does Kazuya teach or even suggest using his polycrystalline silicon isolation structure as a gate. In fact, there is no suggestion in the Kazuya reference to use his isolation structure in an MOS integrated circuit. Therefore, there is no suggestion in the prior art to make the combination suggested by the Examiner. Thus, this proposed combination is improper. "The mere fact that it is possible to find two isolated disclosures which might be combined in such a way to produce a new (invention) does not necessarily render such production obvious unless the art also contains something to suggest the desirability of the proposed combination." (In re Regel, Buchel, and Plempel, 188 USPQ 136 at 139, CCPA 1975). There is no reason why one skilled in the art having the Kazuya reference before him would be tempted to use the polycrystalline silicon isolation structure as part of a gate.

Further, Kazuya's structure is not appropriate for use as a gate. For example, there is no mention of a step whereby the polycrystalline silicon in his groove is doped. In fact, Kazuya teaches that "phosphorus from PSG layer 13 diffuses into polycrystalline silicon layer 18a formed on PSG layer 13 but

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not into polycrystalline silicon layer 18 formed inside recessed region 15. (Kazuya translation, page 12). Thus, Kazuya teaches that the polysilicon in his groove is undoped and thus nonconductive. If one attempted to deposit Kazuya's undoped polysilicon in Applicant's groove, the resulting structure would be inappropriate for use as a gate. For at least the above reasons, one of ordinary skill in the art having the Kazuya reference and Applicant's prior art Figure 2 before him would not find Claims 8 to 16 obvious.

Applicant points out that Claims 8 to 16 include the step of forming conductive material in a groove. As mentioned above, undoped polycrystalline silicon is a very poor conductor. Thus, even if one combined the Kazuya reference with prior art Fig. 2b, the resulting structure still would not teach or render obvious Applicant's claimed invention.

Applicant has added Claim 12 which is similar to Claims 8 and 10 except that certain limitations have been removed. For example, the groove is no longer limited to a rectangular groove. Other minor limitations have been removed as well. Applicant's Claim 12 is patentable for at least the same reasons that Applicant's Claims 8 to 11 are patentable.

Applicant has added Claim 13, directed to a process as in Claim 12, but further comprising a method for electrically contacting the gate. The subject matter set forth in Claim 13 is supported by the above-quoted portion of the specification at page 6, lines 21 to 26. Kazuya fails to teach a method for electrically contacting a polycrystalline silicon isolation region. Thus, Kazuya fails to render obvious Applicant's Claim 13.

Claim 14 is directed to a method whereby the gate is etched below the surface of the source region. Specifically, Claim 14 recites the step of "removing a portion of said

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conductive material in said second, inner groove so that a top portion of said second, inner groove adjacent to said dielectric material is not filled with conductive material. . . ." In contrast, in Kazuya's process "almost none of polycrystalline silicon layer 18 inside recessed region 15 is etched." (Translation, page 13.) Thus, Applicant's Claim 14 is patentable over Kazuya. In the process Kazuya describes as prior art (Figs. 1a to 1d), although polycrystalline silicon is removed from a central portion of Kazuya groove 5, it does not appear that a portion of the polycrystalline silicon in Kazuya groove 5 adjacent to dielectric material 7 is removed. Thus, the process of Claim 14 is patentable over Kazuya Figs. 1a to 1d.

Pursuant to rule 37 C.F.R. 1.56, Applicant wishes to bring U.S. Patents 4,454,646 and 4,454,647 (copies enclosed), each issued to Joy et al. Joy discusses an isolation structure for isolating bipolar transistors formed in an integrated circuit, e.g. as illustrated in Fig. 4 of the '647 patent. The isolation structure includes a polycrystalline silicon-filled groove which extends through an N- epitaxial layer, an N+ buried layer and part of a P- substrate. However, the groove does not extend through a top (third) region having a first conductivity type, a second (middle) region having a second conductivity type, and part of a substrate having said first conductivity type.

"UMOS Transistors on (110) Silicon" by Ammar et al. discusses a structure similar to prior art Figure 2 of the Application. Ammar also illustrates a transistor including a groove and a polycrystalline silicon layer formed across the groove surface (Ammar Figure 11). However, the groove is not filled with polycrystalline silicon. Specifically, Ammar states that he etches the

> U-grooves narrow enough that their surface aperture is sealed by the polysilicon

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deposition. Continuous vapox and metal layers can then be deposited over the U-grooves. A UMOST with a = 1.1 μm is shown in Fig. 11. The polysilicon has sealed up the groove leaving a void.

Applicant's claimed invention is patentable over Ammar because Applicant performs the step of "filling the bottom portion of said second, inner groove with a conductive material so that a top surface of said conductive material . . . lies adjacent to the portion of dielectric material adjacent to said third region . . . ." (Applicant's Claim 12.) Ammar neither teaches or suggests such a step. Instead, Ammar leaves a void or cavity in his groove.

Applicant's Claims 13, 14 and 16 each include the step of removing some of the conductive material in the second, inner groove. Thus, Claim 13 recites the step of "removing part of said second portion of said conductive material . . . ." Claim 14 includes the step of "removing a portion of said conductive material in said second inner groove . . . ." Ammar fails to teach or suggest such a step. Thus, Ammar fails to render obvious Applicant's Claims 13, 14 and 16.

Claim 15 includes the step of "etching said conductive material so that said conductive material on the surface of said third region adjacent to said second, inner groove is removed." Ammar fails to teach or suggest such a step.

As Applicant has overcome each of the Examiner's objections, Applicant respectfully submits that Claims 8 to 16 are in condition for allowance. If the Examiner's next action is other than allowance, the Examiner is respectfully requested to telephone Applicant's attorney at (408) 246-1405.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C., 20231, March 25 -10-
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March 25 1987 Kenneth Leeds
Date of Signature Attorney for Applicant

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